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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,052	07/10/2003	Fredrick D. Fishburn	2003-0076.00/US	6083
7590 01/04/2006			EXAMINER	
Kevin D. Martin			VINH, LAN	
8000 S. Federa	l Way		<u></u>	
MS 01-525			ART UNIT	PAPER NUMBER
Boise, ID 83707-0006			1765	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

			13			
	Application No.	Applicant(s)				
	10/619,052	FISHBURN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Lan Vinh	1765				
 The MAILING DATE of this communication appeariod for Reply 	pears on the cover sheet	with the correspondence add	ress			
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a rep - If NO period for reply is specified above, the maximum statutory period - Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailin earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may by within the statutory minimum of the will apply and will expire SIX (6) Mode, cause the application to become	a reply be timely filed nirty (30) days will be considered timely. DNTHS from the mailing date of this com ABANDONED (35 U.S.C. § 133).	nmunication.			
Status						
1) Responsive to communication(s) filed on 10/1	<u>7/2005</u> .					
2a) ☐ This action is FINAL . 2b) ☑ This	s action is non-final.					
	/_					
closed in accordance with the practice under	Ex parte Quayle, 1935 C.	D. 11, 453 O.G. 213.				
Disposition of Claims						
 4) Claim(s) 1-17 and 21-23 is/are pending in the 4a) Of the above claim(s) is/are withdra 5) Claim(s) 10-17 and 21-23 is/are allowed. 6) Claim(s) 1-4,8 and 9 is/are rejected. 7) Claim(s) 5-7 is/are objected to. 8) Claim(s) are subject to restriction and/o 	wn from consideration.					
· · · · · · · · · · · · · · · · · · ·	or election requirement.					
Application Papers						
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acc		n by the Evaminer				
Applicant may not request that any objection to the		·				
Replacement drawing sheet(s) including the correct		• •	R 1.121(d).			
11)☐ The oath or declaration is objected to by the E			, ,			
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Burea 	ts have been received. ts have been received in ority documents have bee	Application No	tage			
* See the attached detailed Office action for a list Attachment(s)		nt received.				
1) 🔀 Notice of References Cited (PTO-892)		Summary (PTO-413)				
 Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 		o(s)/Mail Date f Informal Patent Application (PTO-1	152)			

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DETAILED ACTION

Response to Amendment/Argument

1. Applicant's arguments, see pages 13-14 of the response, filed 10/17/2005, with respect to rejection of claims 1-5, 8, 10-13, 15-17 under 35 U.S.C 102(e) have been fully considered and are persuasive. The rejection(s) of claims 1-13, 15-17 has been withdrawn. However, upon further consideration, a new ground of rejection of claims 1-4, 8 is made based on previously cited reference of Chiang et al (US 6,383,863). A discussion of the rejection follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-4, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang et al (US 6.383,863)

Chiang discloses a method for forming a salicide layer. The method comprises the steps of:

forming a first conductive layer 4 and one dielectric layer 5 on the first conductive layer (col 3, lines 7-14)

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forming a patterned mask layer 8 over the at least one dielectric layer and overlying the first conductive layer (col 3, lines 18-20)

etching the dielectric layer 5 and the first conductive layer 4 using the mask as a pattern to form first and second cross-sectional sidewalls from the dielectric layer and the first conductive layer 4 (col 3, lines 20-22; fig. 2)

forming a first dielectric spacer 10 on the first sidewall and a second dielectric spacer 10 on the second sidewall, where an upper surface of sidewall is above an upper surface of the first and second spacers (col 3, lines 37-39; fig. 8)

forming a second conductive layer over the at least one dielectric layer and over the first conductive layer (col 4, lines 25-27)

removing the second conductive layer from over the first conductive layer and leaving the second conductive layer at other locations (col 4, lines 30-35; fig. 6) etching the at least one dielectric layer to expose the first conductive layer 4 (col 4, lines 55-60, fig. 8)

forming a silicide layer simultaneously on the first and second conductive layers (col 5, lines 3-9; fig. 9)

Regarding claim 2, Chiang discloses etching of the dielectric layer to expose the first conductive layer is performed in the absence of a mask (col 4, lines 55-60)

Regarding claim 3, Chiang discloses the etch of the first conductive layer defines a plurality of transistor control gates (fig. 2)

Regarding claim 4, Chiang discloses that the removal of the second conductive layer from over the first conductive layer defines a plurality of conductive plugs which contact a semiconductor wafer (col 4, lines 35-40; fig. 6)

Regarding claim 8, Chiang discloses forming the first polysilicon layer 4 and second polysilicon layer 18 (col 3, lines 4-5; col 4, lines 36-37), forming a cobalt layer and heating the cobalt layer to form a silicide layer (col 5, lines 1-10), etching to remove the unreacted metal layer leaving a majority of the silicide layer (col 5, lines 10-15)

Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (US 6,383,863) in view of Shin et al (US 6,635,536)

Chiang method has been described above. Unlike the instant claimed inventions as per claim 9, Chiang fails to disclose forming the spacer from aluminum oxide

Shin, in a method for manufacturing semiconductor device, discloses forming a spacer of SiN or aluminum oxide (col 2, lines 33-35)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Chiang method by forming the spacer from aluminum oxide because

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according to Shin, the spacer on a transistor can be formed of SiN or aluminum oxide film (col 2, lines 8-35)

Allowable Subject Matter

8. Claims 5-7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The rejection of claim 5 has been withdrawn as discussed above in paragraph 1

The statement of reasons for the indication of allowable subject of claims 6-7 have been stated in the previous office action

Claims 10-17, 21-23 allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 10, 15, the cited prior art of record fails to disclose or suggest a method for forming a semiconductor device comprises the steps of planarizing the blanket polysilicon plug layer to remove the plug layer from over the plurality of transistor word lines to form a plurality of polysilicon plugs and to expose the at least one dielectric layer/ removing a portion of the blanket conductive plug layer by planarizing the blanket conductive plug layer in the absence of a mask layer to form a plurality of conductive plugs, in combination with the rest of the limitations of claims 10, 15

The reasons for allowance of claim 21 has been stated in the previous office action

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Response to Arguments/Reasons to maintain rejection of claim 1 based on Chiang (US 6,383,863)

9. The applicants argue that Chiang fails as a reference under 35 U.S.C 102(e) at least because layer 11 does not contact sidewall formed by layer 4 and 6. This argument is moot in view of the new ground(s) of rejection because as discussed in paragraph 3 above, Chiang discloses forming a first dielectric spacer 10 on/contacting the first sidewall and the second sidewall formed by layers 4 and 5

The applicants argue that, in Chiang, the upper surface of the sidewall provided by conductive layer 4 (dielectric layer 6 has been etched removed at this point) still is not above an upper surface of the spacer provided by FIG. 11. This argument is moot in view of the new ground(s) of rejection because as discussed in paragraph 3 above, an upper surface of sidewall of layer 5 is above an upper surface of the first and second spacers (fig. 8)

The applicants argue that the recitation from claim 1 of "removing the second conductive layer from over the first conductive layer" which results in the silicidation of the first conductive layer over its entire width is useful, novel, and nonobvious over Chiang. This argument is unpersuasive because it does not commensurate with the scope of claim 1 since claim 1 does not recite/require "removing the second conductive layer from over the first conductive layer" which results in the silicidation of the first conductive layer over its entire width.

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Conclusion

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10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 19, 2005